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EXAMINER	
WARD, ERIC A	

ART UNIT	PAPER NUMBER
2891	

MAIL DATE	DELIVERY MODE
07/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,969	ALBRECHT ET AL.	
	Examiner	Art Unit	
	ERIC WARD	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/30/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 4, 14, and 16 objected to because of the following informalities:

Claim 4 recites “the semiconductor substrate (1) facing away" and should be -- the semiconductor substrate facing away--.

Claim 14 depends on Claim 13 which depends on Claim 11 which depends on Claim 1. However, Claim 14 recites “from which the second contact metallization” which lacks antecedent basis in Claims 1, 11 and 13. Claim 14 should properly depend upon Claim 4.

Claim 16 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. See Claim Rejections 35 USC § 112.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 16 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 16, which depends upon Claim 1, recites the limitation “wherein n doping and p doping of the semiconductor layers are exchanged for one another” which is indefinite since Claim 1 recites the limitation “wherein an area of n-doped semiconductor layers and an area of p-doped semiconductor layers” and further recites structure “wherein the area of the p-doped semiconductor layers is provided in the protective diode section on the side facing away from the first pn junction with an n-doped semiconductor layer." Specifically, Claim 16 is inconsistent with Claim 1 since Claim 1 recites limitations to specific doping profiles which cannot be reversed in dependent claims.

Furthermore, for a given doping profile of Claim 1, Claim 16 fails to further limit Claim 1 but instead broadens it to include reverse doping profiles.

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3,5-8,11-14,16-18 rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Jiang et al. (US 6,185,240) (henceforth Jiang) in view of Sawai et al. (JP 57093591 Abstract) (henceforth Sawai).

Regarding **Claim 1** insofar as definite, Jiang discloses a light-emitting semiconductor component (title) comprising:

a) a monolithically produced sequence of semiconductor layers (Fig. 1 items 109,111,119) (Col. 2 Lines 25-28),

b) wherein an area of n-doped semiconductor layers (Fig. 1 item 109) and

c) an area of p-doped semiconductor layers (Fig. 1 item 119) follow one another and

d) a first pn junction is formed between the n-doped areas and p-doped areas (Fig. 1 item 111, specifically item 115) (Col. 2 Lines 26-27), wherein the first pn junction is subdivided into

e) a light-emitting section (Fig. 1 item 103 defined by trench 131) (Col. 2 Lines 34-35) and

f) a protective-diode section (Fig. 1 item 105 defined by trench 133) (Col. 2 Line 42) by

g) an insulating section (Fig. 1 item 133),

h) wherein the insulating section electrically insulates the light-emitting section (i.e. disposed to the left of the insulating section) and the protective-diode section (i.e. to the right of the insulating section) from one another in the area of the p-doped semiconductor layers,

i) wherein the area of the p-doped semiconductor layers is provided in the protective-diode section on the side facing away from the first pn junction (i.e. disposed to the right) with an n-doped semiconductor layer (Fig. 1 item 109) which forms a second pn junction (see attached below) with the area of p-doped semiconductor layers in the protective-diode section and is electrically

conductively connected to the area of p-doped semiconductor layers (through Fig. 1 item 123 conductive layer) in the light-emitting section, and

j) wherein the first pn junction has a larger area (Fig. 2 item 105) (Fig. 1 trench 133 has a width from between 0.1 to 100 microns) in the protective-diode section than in the light-emitting section (Fig. 2 item 122) (Fig. 1 trench 131 has a width from between 0.1 to 100 microns, thereby inclusive of instances wherein the protective-diode section has a larger area).

Should Jiang be so narrowly construed as to fail to disclose a second pn junction, then it would have been obvious at the time of the invention to one having ordinary skill in the art to have incorporated a second PN junction (i.e. forming an NPN junction) as taught by Sawai in the device of Jiang in order to regulate the surge rate during breakdown (Sawai abstract).

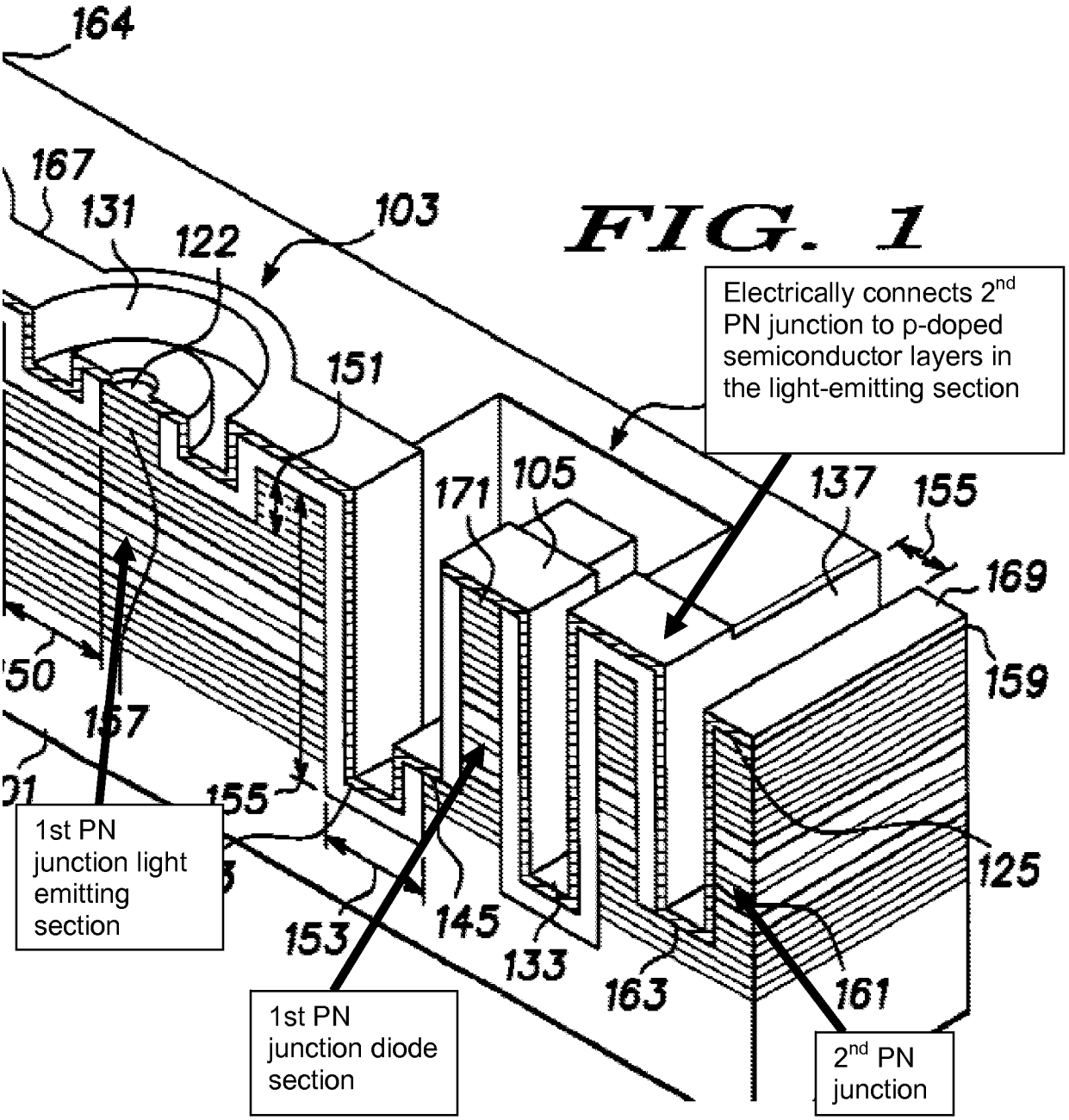

FIG. 1

Regarding **Claim 2**, Jiang further discloses wherein the area of the first pn junction is larger in the protective-diode section than in the light-emitting section by at least a factor of 100 (Col. 2 Lines 59-67, trench defining VCSEL ranges from 0.1 to 100 microns and

trench defining diode ranges from 0.1 to 100 microns, thereby covering the range wherein the protective diode section has an area greater by at least a factor of 100).

Regarding **Claim 3**, Jiang further discloses wherein the sequence of semiconductor layers is applied to a semiconductor substrate (Fig. 1 item 101) (Col. 1 Lines 66-67).

Regarding **Claim 5**, Jiang further discloses wherein the area of n-doped semiconductor layers (Fig. 1 item 109) is only partially interrupted by the insulating section (Fig. 1 item 133).

Regarding **Claim 6**, Jiang further discloses wherein the insulating section (Fig. 1 item 133) extends from a surface of the sequence of semiconductor layers opposite to the semiconductor substrate into the area of n-doped layers (Fig. 1 item 109).

Regarding **Claim 7**, Jiang further discloses wherein the light-emitting section is formed by a vertical cavity surface emitting laser (VCSEL) (Col. 1 Lines 57-60).

Regarding **Claim 8**, Jiang further discloses wherein the first pn junction (Fig. 1 item 111) is arranged between a first sequence of Bragg reflector layers (Fig. 1 item 109) and a second sequence of Bragg reflector layers (Fig. 1 item 119), each of which has a multiplicity of layer pairs (as pictured), and the two sequences of Bragg reflector layers form a laser resonator (VCSEL, Col. 1 Lines 57-60), one of the two sequences of the

Bragg reflector layers (Fig. 1 item 119) being semitransparent for the laser radiation generated in the pn junction (in order to output light through Fig. 1 item 122) (Col. 2 Lines 38-41).

Regarding **Claim 11**, Jiang further discloses wherein the insulating section (Fig. 1 item 133) is constructed as trench (Col. 2 Line 31).

Regarding **Claim 12**, Jian further discloses wherein the light-emitting section and the protective-diode section have a mesa-shaped structure (formed through lithography and etching) (Col. 2 Lines 30-33) on the side of the trench.

Regarding **Claim 13**, Jiang further discloses wherein the trench (Fig. 1 item 133) is bounded by areas which are provided with an insulating layer (Fig. 1 item 121) (Col. 2 Line 8).

Regarding **Claim 14**, Jiang further discloses wherein the trench (Fig. 1 item 133) is filled with a material from which a contact metallization (Fig. 2 items 123,125) is formed.

Regarding **Claim 16** insofar as definite, Jiang discloses n doping and p doping of the semiconductor layers. Furthermore, it would have been obvious at the time of the invention to reverse the doping order as is well-known in the art.

Regarding **Claim 17**, Jiang discloses a light-emitting semiconductor component comprising:

a) a monolithically produced sequence of semiconductor layers (Fig. 1 items 109,111,119) (Col. 2 Lines 25-28),

b) wherein an area of n-doped semiconductor layers (Fig. 1 item 109) and

c) an area of p-doped semiconductor layers (Fig. 1 item 119) follow one another and

d) a first pn junction (Fig. 1 item 111, specifically item 115) (Col. 2 Lines 26-27) is formed between the areas,

e) wherein the first pn junction is subdivided into a light-emitting section (Fig. 1 item 103 defined by trench 131) (Col. 2 Lines 34-35) and

f) a protective-diode section (Fig. 1 item 105 defined by trench 133) (Col. 2 Line 42) by

g) an insulating section (Fig. 1 item 133),

h) wherein the insulating section electrically insulates the light-emitting section (i.e. disposed to the left of the insulating section) and the protective-diode section (i.e. to the right of the insulating section) from one another in the area of the p-doped semiconductor layers,

i) wherein the area of the p-doped semiconductor layers is provided in the protective-diode section on the side facing away from the first pn junction (i.e. to the right of the first pn junction) with an n-doped semiconductor layer (Fig. 1 item 109) which forms a second pn junction (see attached Claim 1) with the area of p-

doped semiconductor layers (Fig. 1 item 119) in the protective-diode section (i.e. to the right of insulating section) and is electrically conductively connected (through Fig. 1 item 123 conductive layer) to the area of p-doped semiconductor layers in the light-emitting section, and

j) wherein the first pn junction in the area of the protective-diode section is short circuited (Fig. 1 item 169 short circuits first pn junction, as shown in Applicants' Fig. 1).

Should Jiang be so narrowly construed as to fail to disclose a second pn junction, then it would have been obvious at the time of the invention to one having ordinary skill in the art to have incorporated a second PN junction (i.e. forming an NPN junction) as taught by Sawai in the device of Jiang in order to regulate the surge rate during breakdown (Sawai abstract).

Regarding **Claim 18**, Jiang further discloses wherein an electrically conductive layer (Fig. 1 item 169) is applied to a side edge (inside right edge of Fig. 1 trench 137) of the sequence of semiconductor layers facing the protective-diode section and electrically connects the area of n-doped semiconductor layers and the area of p-doped semiconductor layers with one another.

Claim 4,9, and 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US 6,185,240) (henceforth Jiang) as applied to Claims above, further in view of Dowd et al (US 6,639,931) (henceforth Dowd).

Regarding **Claim 4**, Jiang further discloses a first contact metallization (Fig. 1 item 123) applied to a side of the semiconductor substrate and a second contact metallization (Fig. 1 item 125) (Col. 3 Lines 46-49) applied to part-areas of a surface of the sequence of semiconductor layers on to the semiconductor substrate.

Jiang fails to expressly teach wherein the first contact metallization is applied to a side of the semiconductor substrate facing away from the sequence of semiconductor layer (i.e. Jiang teaches a lateral contact structure rather than a back lower contact) (Col. 3 Line 65 to Col. 4 Line 6).

Dowd teaches forming a back lower contact (Fig. 2 item 8) (Col. 1 Line 15).

It would have been obvious at the time of the invention to one having ordinary skill in the art to have formed the device of Jiang with a back contact as taught by Dowd in order to make use of the back-side of the substrate leading to a more compact device.

Regarding **Claim 9**, Jiang fails to expressly teach wherein in one of the two sequences of Bragg reflector layers, at least one current aperture is provided for spatially limiting an operating current flowing through the first pn junction in the light-

emitting section during the operation of the vertical cavity surface emitting laser. Jiang omits some engineering details (Col. 2 Lines 15-18).

Dowd teaches wherein a typical VCSEL, one of the two sequences of Bragg reflector layers (Fig. 2 items 4 and 5) (Col. 1 Lines 7-21) includes a current aperture (Fig. 2 item 9) is provided for spatially limiting an operating current flowing through the first pn junction in a light-emitting section during the operation of a vertical cavity surface emitting laser.

It would have been obvious at the time of the invention to one having ordinary skill in the art to have included a current aperature as taught by Dowd in order to create a functional and operating VCSEL (Dowd Col. 1 Lines 10-12).

Regarding **Claim 10**, Jiang further discloses wherein the second contact metallization (Fig. 2 item 123) partially covers the surface of the light-emitting section (Fig. 1 and Fig. 2 item 122) in such a manner that an uncovered area remains as light exit opening.

Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US 6,185,240) (henceforth Jiang `240) in view of Jiang et al. (US 5,757,836) (henceforth Jiang `836).

Jiang `240 fails to expressly teach wherein the insulating section is formed by an implantation, diffusion or oxidation process.

Jiang `836 teaches a VCSEL having an insulating section (Fig. 2 and 3 items 51 and 52) (Col. 3 Lines 57-67) forming insulating sections by an implantation process.

It would have been obvious at the time of the invention to one having ordinary skill in the art to have modified the device of Jiang `240 with the implant isolation regions as taught by Jiang `836 in order to effectively insulate VCSELs from adjacent components as well as absorb spontaneous lateral emission (Jiang `836 Col. 4 Lines 4-9).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC WARD whose telephone number is (571)270-3406. The examiner can normally be reached on M-T 5:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 5712721722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EAW/

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